

716	8	Subclass
Class		
ISSUE CLASSIFICATION		

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PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

SCANNED 6/13 Q.A. 63

APPLICATION NO. 09/B43486	CONT/PRIOR	CLASS 716	SUBCLASS 8	ART UNIT 2825 2811	EXAMINER Q. Vn
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APPLICANTS

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TITLE

Optimal simultaneous design and floorplanning of integrated circuits

PTO-2040
12/89

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drawn <i>5</i>	Figs. Drawn <i>7</i>	Print Figs. <i>4</i>	Total Claims <i>24</i>	Print Claim for O.G. <i>1</i>
The term of this patent subsequent to _____ (date) has been disclaimed.	<i>Quang Vu</i> (Assistant Examiner)			NOTICE OF ALLOWANCE MAILED <i>06/01/04</i>	
	<i>OR</i> <i>NADAV</i> (Primary Examiner)			ISSUE FEE Amount Due <i>\$ 1630</i>	
The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	<i>ORI NADAV</i> (Primary Examiner)			Date Paid	
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The terminal _____ months of this patent have been disclaimed.	<i>Julien Miller</i> (Legal Instruments Examiner)			ISSUE BATCH NUMBER	
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